COMPLETE LISTING OF CLAIMS

Claim 1 (currently amended) A current switch comprising:

a differential pair of transistors ~~Q1 and Q2~~;

a pair of cascode transistors ~~QA and QB~~ respectively coupled to said differential pair of transistors ~~Q1 and Q2, respectively~~; and

first means for maintaining said cascode transistors ~~QA and QB~~ in an 'on' state regardless of the states of ~~Q1 and Q2~~ said differential pair of transistors, said first means includes a first and a second current source adapted to supply a first and second trickle current to said pair of cascode transistors,

a third current source adapted to supply a third current to the common emitters of said differential pair of transistors,

wherein said first and second trickle currents are approximately 10 to 100 times smaller than said third current.

Claims 2-3 (canceled).

Claim 4 (currently amended) The invention of Claim 1 ~~Claim 3~~ wherein said first and second current sources are respectively coupled to the emitters of said pair of cascode transistors ~~QA and QB, respectively~~.

Claim 5 (currently amended) The invention of Claim 1 ~~Claim 3~~ wherein said first and second trickle currents are approximately equal.

Claim 6 (currently amended) The invention of Claim 1 wherein the emitters of said pair of cascode transistors ~~QA and QB~~ are coupled to the collectors of said differential pair of transistors ~~Q1 and Q2~~, respectively.

Claim 7 (currently amended) The invention of Claim 1 wherein the collectors of said ~~QA and QB~~ are coupled to first and second outputs, respectively.

Claim 8 (currently amended) The invention of Claim 1 wherein the bases of said pair of cascode transistors ~~QA and QB~~ are connected in common to a voltage potential ~~source VREF4~~.

Claims 9-13 (canceled)

Claim 14 (currently amended) The invention of Claim 1 ~~Claim 12~~ wherein said current switch further includes second means for supplying a pair of complementary input signals ~~Bn and Bn~~.

Claim 15 (currently amended) The invention of Claim 14 wherein said differential pair of transistors ~~Q1 and Q2~~ are adapted to couple said third current to a collector ~~either the collector of Q1 or the collector of Q2~~ in response to said pair of complementary input signals ~~Bn and Bn~~.

Claim 16 (currently amended) The invention of Claim 15 wherein the bases of said differential pair of transistors ~~Q1 and Q2~~ are respectively coupled to said pair of complementary input signals ~~Bn and Bn~~.

Claim 17 (currently amended) The invention of Claim 1 ~~Claim 12~~ wherein said current switch further includes a buffer transistor ~~Q5~~ connected between said third current source and the common emitters of said differential pair of transistors ~~Q1 and Q2~~.

Claim 18 (currently amended) The invention of Claim 17 wherein the base of ~~Q5~~ said buffer transistor is coupled to a second voltage potential ~~supply VREF2~~.

Claim 19 (original) The invention of Claim 14 wherein said second means includes a driver circuit.

Claim 20 (currently amended) The invention of Claim 19 wherein said driver circuit includes a current switch comprising:

a fourth current source for supplying a fourth current;

a second differential pair of transistors ~~Q10 and Q11~~ adapted to couple said fourth current to either ~~the~~ a collector of ~~Q10 or the collector of Q11~~ of said second differential pair of transistors in response to a second pair of complementary input signals ~~Xn and Xn~~;

a second pair of cascode transistors ~~Q14 and Q15~~ having emitters respectively coupled to the collectors of said second differential pair of transistors ~~Q10 and Q11, respectively~~; and

fifth and sixth current sources adapted to supply trickle currents to the emitters of said second pair of cascode transistors ~~Q14 and Q15, respectively~~, in order to maintain said second pair of cascode transistors ~~Q14 and Q15~~ in an 'on' state regardless of the states of said second differential pair of transistors ~~Q10 and Q11~~.

Claim 21 (currently amended) The invention of Claim 20 wherein said driver circuit further includes two transistors ~~Q12 and Q13~~ having bases respectively coupled to the collectors of said second pair of cascode transistors ~~Q14 and Q15, respectively, collectors coupled to ground, and emitters coupled to outputs Bn and Bn, respectively~~.

Claim 22 (currently amended) A current switch comprising:

a first current source for supplying a first current;

a differential pair of transistors ~~Q1 and Q2~~ adapted to couple said first current to one of the collectors of said differential pair of transistors ~~either the collector of Q1 or the collector of Q2~~ in response to a pair of complementary input signals ~~Bn and –Bn~~;

a pair of cascode transistors ~~QA and QB~~ having emitters respectively coupled to the collectors of said differential pair of transistors ~~Q1 and Q2, respectively~~; and

second and third current sources adapted to respectively supply first and second trickle currents to the respective emitters of said pair of cascode transistors ~~QA and QB, respectively,~~ in order to maintain said pair of cascode transistors ~~QA and QB~~ in an 'on' state regardless of the states of said differential pair of transistors, ~~Q1 and Q2~~.

wherein said trickle currents are approximately 10 to 100 times smaller than said first current

Claims 23-27 (canceled)

Claim 28 (currently amended) A digital to analog converter comprising:

a first current summing bus;

a second current summing bus; and

a plurality of current switches, each switch including:

a first current source for supplying a first current;

a differential pair of transistors ~~Q1 and Q2~~ adapted to couple said first current to either the first current summing bus or the second current summing bus in response to a pair of complementary input signals ~~Bn and Bn~~;

a pair of cascode transistors ~~QA and QB~~ having emitters respectively coupled to the collectors of said differential pair of transistors ~~Q1 and Q2, respectively~~, and collectors coupled to said first and second current summing buses, respectively; and

second and third current sources adapted to respectively supply first and second trickle currents to the emitters of said pair of cascode transistors ~~QA and QB, respectively,~~ in order to maintain said pair of cascode transistors ~~QA and QB~~ in an 'on' state regardless of the states of said differential pair of transistors, ~~Q1 and Q2~~.

wherein the trickle currents are approximately 10 to 100 times smaller than said first current.

Claim 29 (currently amended) The invention of Claim 28 wherein the bases of said pair of cascode transistors ~~QA and QB~~ are connected in common to a voltage potential ~~source VREF4~~.

Claims 30-32 (canceled)

Claim 33 (currently amended) The invention of Claim 28 wherein each current switch further includes a buffer transistor ~~Q5~~ connected between said first current source and the common emitters of differential pair of transistors ~~Q1 and Q2~~.

Claim 34 (canceled)

Claim 35 (original) The invention of Claim 28 wherein said first and second trickle currents are approximately equal.

Claim 36 (canceled)

Claim 37 (currently amended) The invention of Claim 28 wherein each current switch further includes a driver circuit for supplying said pair of complementary input signals ~~Bn and Bn~~.

Claim 38 (currently amended) The invention of Claim 37 wherein said driver circuit includes:

a fourth current source for supplying a fourth current;

a second differential pair of transistors ~~Q10 and Q11~~ adapted to couple said fourth current to ~~either the collector of Q10 or the collector of Q11~~ one of the collectors of said second differential pair of transistors in response to a second pair of complementary input signals ~~Xn and Xn~~;

a second pair of cascode transistors ~~Q14 and Q15~~ having emitters respectively coupled to the collectors of said second differential pair of transistors ~~Q10 and Q11, respectively~~;

fifth and sixth current sources adapted to respectively supply third and fourth trickle currents to the emitters of said second pair of cascode transistors ~~Q14 and Q15, respectively,~~ in order to maintain said second pair of cascode transistors ~~Q14 and Q15~~ in an 'on' state regardless of the states of said second differential pair of transistors ~~Q10 and Q11~~; and

two transistors ~~Q12 and Q13~~ having bases respectively coupled to the collectors of said second pair of cascode transistors ~~Q14 and Q15, respectively~~, and emitters adapted to output said pair of complementary input signals ~~voltages Bn and Bn, respectively~~.

Claim 39 (currently amended) The invention of Claim 38 wherein said fourth current and said third and fourth trickle currents are chosen to generate a low output voltage swing at the emitters of said two transistors having bases respectively coupled to the collectors of said second pair of cascode transistors ~~Q12 and Q13~~.

Claim 40 (canceled)